Remarks:

Reconsideration of the application is requested.

Claims 1-3 and 5-9 are now in the application. Claims 1 and 5 have been amended. Claim 4 has been canceled.

In item 2 of the Office action, the Examiner rejected claims 1-3 and 5-10 as being fully anticipated by Sasaki et al. (U.S. 4,833,395) under 35 U.S.C. § 102(b). However, in item 10, the Examiner objected to claim 4 but indicated that it contained allowable subject matter. Accordingly, claim 1 has been amended to include the features of claim, while claim 4 has been canceled. Claim 1 contains allowable subject matter and should be allowed. Claims 2-3 and 5-9 depend on claim 1 and are also now allowable. Claim 5 has been amended to conform to amended claim 1.

In view of the foregoing, reconsideration and allowance of claims 1-3 and 5-9 are solicited. In the event the Examiner should still find any of the claims to be unpatentable, please telephone counsel so that patentable language can be substituted.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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October 3, 2001

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Version with Markings to Show Changes:

In the Claims:

Cancel claim 4.

Claim 1 (amended). An integrated semiconductor circuit, comprising:

[at least one] a plurality of pad [cell] cells to be monitored in one operating mode by a functional test, said [at least one] plurality of pad [cell] cells each having a connecting pad, an upstream output driver, and a connection for an input signal; [and]

a signal transmitter for producing periodic signal sequences, said signal transmitter having a connection for a periodic output signal connected to said connection for an input signal of said [at least] plurality of pad [cell] cells to be tested, in order to test a transmission response of said [at least one] plurality of pad [cell] cells in said one operating mode; and

shift register cells each connected in series between said connection for an input signal of a respective one of said plurality of pad cells and said connection of said signal transmitter for an output signal.

Claim 5 (amended). The integrated semiconductor circuit according to claim 1, [wherein said at least one pad cell to be tested is a plurality of pad cells, and] <u>including</u> multiplexer circuits [are] each connected between said connection for an input signal of a respective one of said pad cells and said connection of said signal transmitter for an output signal, to switch over between said one operating mode and another operating mode.